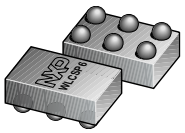


BGS8M4UK

SiGe:C Low Noise Amplifier MMIC with bypass switch for LTE

Rev. 1 — 1 December 2015 Product data sheet

1. Product profile

1.1 General description

The BGS8M4UK is a Low Noise Amplifier (LNA) with bypass switch for LTE receiver applications, available in a Wafer Level Chip-Scale Package (WLCSP). The BGS8M4UK requires one external matching inductor.

The BGS8M4UK delivers system-optimized gain for both primary and diversity applications where sensitivity improvement is required. The high linearity of this low noise device ensures the required receive sensitivity independent of cellular transmit power level in Frequency Division Duplex (FDD) systems. When receive signal strength is sufficient, the BGS8M4UK can be switched off to operate in bypass mode at a 1 μA current, to lower power consumption. The BGS8M4UK requires only one external matching inductor.

The BGS8M4UK is optimized for 1805 MHz to 2200 MHz.

1.2 Features and benefits

- Operating frequency from 1805 MHz to 2200 MHz
- Noise figure (NF) = 0.8 dB
- Gain 16.6 dB
- High input 1 dB compression point of −6.5 dBm
- Bypass switch insertion loss of −2.7 dB
- High in band $IP3_i$ of −0.5 dBm
- Supply voltage 1.5 V to 3.1 V
- Integrated supply decoupling capacitor
- Optimized performance at a supply current of 4.4 mA
- Bypass mode current consumption < 1 μA
- Integrated temperature stabilized bias for easy design
- Requires only one input matching inductor
- Input and Output AC coupled
- ESD protection on all pins (HBM > 2 kV)
- Integrated matching for the output
- Extremely small Wafer Level Chip-Scale Package (WLCSP)
  6 bumps; 0.69 mm × 0.44 mm × 0.29 mm; 0.25 mm / 0.26 mm bump pitch
- 180 GHz transit frequency - SiGe:C technology
- Moisture sensitivity level of 1

1.3 Applications

- LNA for LTE reception in smart phones, feature phones, tablet PCs and RF front-end modules.

1.4 Quick reference data

Table 1. Quick reference data

f = 1960 MHz; V_{CC} = 2.8 V; $V_{I(CTRL)} \geq 0.8$ V; T_{amb} = 25 °C; input matched to 50 Ω using a 4.7 nH inductor in series; see Figure 4 unless otherwise specified.

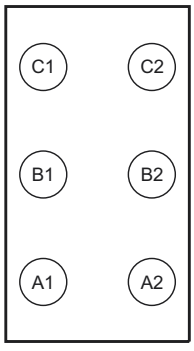
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.5	-	3.1	V
I_{CC}	supply current	in gain mode	-	4.4	-	mA
		in bypass mode; 0.1 V ≤ $V_{I(CTRL)}$ ≤ 0.3 V	-		1	μA
G_p	power gain	in gain mode [1]	-	16.6	-	dB
		in bypass mode [1]	-	–2.7	-	dB
NF	noise figure	[1][2]	-	0.8	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression	[1]	-	–6.5	-	dBm
$IP3_i$	input third-order intercept point	[1]	-	–0.5	-	dBm

[1] E_UTRA operating band 2 (1930 MHz to 1990 MHz).

[2] PCB losses are subtracted.

2. Pinning information

2.1 Pinning



Bump side view

Fig 1. Bump mapping

2.2 Pin description

Table 2. Ball description

Symbol	Pad	Description
GND	A1	ground
V_{CC}	B1	supply voltage
RF_OUT	C1	RF out
CTRL	A2	gain control, switch between gain and bypass mode
RF_IN	B2	RF in
GND_RF	C2	ground RF

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BGS8M4UK	WLCSP6	wafer level chip-scale package; 6 bumps; 0.69 × 0.44 × 0.29 mm	SOT1445-1

4. Marking

Table 4. Marking codes

Type number	Marking code
BGS8M4UK	single character, indicating assembly month.[1]

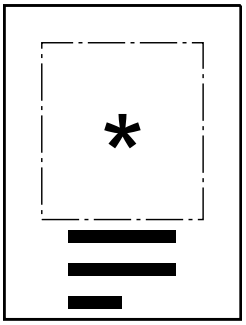
[1] Month code see Table 5.

Table 5. Calender marking month code

Asterisk (*) is replaced by character in table, see Figure 2.

Year [1]	Month											
	J	F	M	A	M	J	J	A	S	O	N	D
2015	A	B	C	D	E	F	G	H	I	J	K	L
2016	M	N	O	P	Q	R	S	T	U	V	W	X
2017	Y	Z	b	d	f	h	3	4	5	6	7	8

[1] Rotates every 3 years.



Pin A1 location: the marking stripes below character indicate the side where pin A1 is located.

Fig 2. Marking code description

5. Block diagram

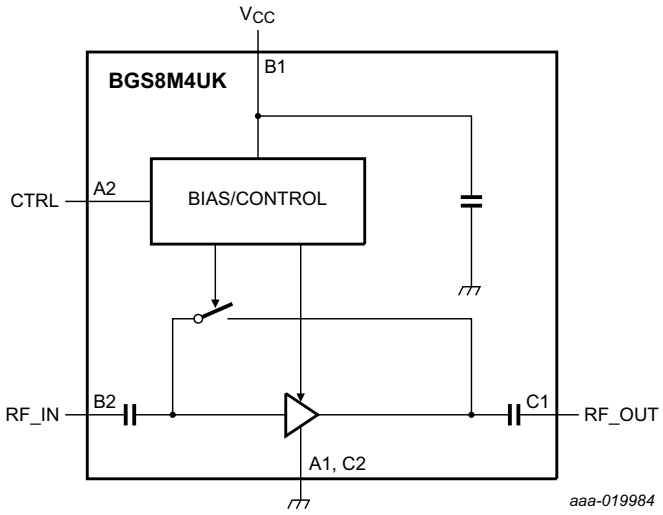


Fig 3. Block diagram

6. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Absolute Maximum Ratings are given as Limiting Values of stress conditions during operation, that must not be exceeded under the worst probable conditions.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	[1]	−0.5	+5.0	V
$V_{I(CTRL)}$	input voltage on pin CTRL	$V_{I(CTRL)} < V_{CC} + 0.6$ V [1][2]	−0.5	+5.0	V
$V_{I(RF\_IN)}$	input voltage on pin RF_IN	DC, $V_{I(RF\_IN)} < V_{CC} + 0.6$ V [1][2][3]	−0.5	+5.0	V
$V_{I(RF\_OUT)}$	input voltage on pin RF_OUT	DC, $V_{I(RF\_OUT)} < V_{CC} + 0.6$ V [1][2][3]	−0.5	+5.0	V
P_i	input power	[1]	-	10	dBm

Table 6. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).
Absolute Maximum Ratings are given as Limiting Values of stress conditions during operation, that must not be exceeded under the worst probable conditions.

Symbol	Parameter	Conditions	Min	Max	Unit
P_{tot}	total power dissipation	$T_{sp} \leq 130$ °C	-	55	mW
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		-	150	°C
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM) According to ANSI/ESDA/JEDEC standard JS-001	-	±2	kV
		Charged Device Model (CDM) According to JEDEC standard JESD22-C101C	-	±1	kV

[1] Stressed with pulses of 200 ms in duration.

[2] Warning: due to internal ESD diode protection, the applied DC voltage shall not exceed V_{CC} + 0.6 V and shall not exceed 5.0 V in order to avoid excess current.

[3] The RF input and output are AC coupled through internal DC blocking capacitors.

7. Recommended operating conditions

Table 7. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.5	-	3.1	V
T_{amb}	ambient temperature		−40	+25	+85	°C
$V_{I(CTRL)}$	input voltage on pin CTRL	bypass mode	-	-	0.25	V
		ON state	0.8	-	-	V

8. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j\text{-}sp)}$	thermal resistance from junction to solder point		225	K/W

9. Characteristics

Table 9. Characteristics

1805 MHz ≤ f ≤ 2200 MHz; V_{CC} = 1.8 V; $V_{I(CTRL)} \geq 0.8$ V; T_{amb} = 25 °C; input matched to 50 Ω using a 4.7 nH inductor in series; see Figure 4 unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gain mode						
I_{CC}	supply current	$V_{I(CTRL)} \geq 0.8$ V	-	4.1	-	mA
G_p	power gain	f = 1843 MHz [1]	-	16.7	-	dB
		f = 1960 MHz [2]	-	16.3	-	dB
		f = 2140 MHz [3]	-	15.4	-	dB

Table 9. Characteristics *...continued*

1805 MHz ≤ f ≤ 2200 MHz; V_{CC} = 1.8 V; $V_{I(CTRL)}$ ≥ 0.8 V; T_{amb} = 25 °C; input matched to 50 Ω using a 4.7 nH inductor in series; see Figure 4 unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
RL_{in}	input return loss	f = 1843 MHz	[1]	-	6.0	-	dB
		f = 1960 MHz	[2]	-	7.0	-	dB
		f = 2140 MHz	[3]	-	9.0	-	dB
RL_{out}	output return loss	f = 1843 MHz	[1]	-	15	-	dB
		f = 1960 MHz	[2]	-	11	-	dB
		f = 2140 MHz	[3]	-	8	-	dB
ISL	isolation	f = 1843 MHz	[1]	-	25	-	dB
		f = 1960 MHz	[2]	-	25	-	dB
		f = 2140 MHz	[3]	-	25	-	dB
NF	noise figure	f = 1843 MHz	[1][4]	-	0.8	-	dB
		f = 1960 MHz	[2][4]	-	0.8	-	dB
		f = 2140 MHz	[3][4]	-	0.85	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression	f = 1843 MHz	[1]	-	−11.0	-	dBm
		f = 1960 MHz	[2]	-	−10.5	-	dBm
		f = 2140 MHz	[3]	-	−9.5	-	dBm
$IP3_i$	input third-order intercept point	f = 1843 MHz	[1]	-	−2.0	-	dBm
		f = 1960 MHz	[2]	-	−1.0	-	dBm
		f = 2140 MHz	[3]	-	−1.5	-	dBm
t_{on}	turn-on time	time from $V_{I(CTRL)}$ ON, to 90 % of the gain		-	-	4	µs
t_{off}	turn-off time	time from $V_{I(CTRL)}$ OFF, to 10 % of the gain		-	-	1	µs
Bypass mode							
I_{CC}	supply current	$V_{I(CTRL)}$ < 0.3 V		-	-	1	µA
G_p	power gain	f = 1843 MHz	[1]	-	−2.8	-	dB
		f = 1960 MHz	[2]	-	−2.9	-	dB
		f = 2140 MHz	[3]	-	−3.1	-	dB
RL_{in}	input return loss	f = 1843 MHz	[1]	-	14	-	dB
		f = 1960 MHz	[2]	-	13	-	dB
		f = 2140 MHz	[3]	-	12	-	dB
RL_{out}	output return loss	f = 1843 MHz	[1]	-	9.0	-	dB
		f = 1960 MHz	[2]	-	8.5	-	dB
		f = 2140 MHz	[3]	-	8.0	-	dB

[1] E_UTRA operating band 3 (1805 MHz to 1880 MHz).

[2] E_UTRA operating band 2 (1930 MHz to 1990 MHz).

[3] E_UTRA operating band 1 (2110 MHz to 2170 MHz).

[4] PCB losses are subtracted

Table 10. Characteristics

1805 MHz ≤ f ≤ 2200 MHz; V_{CC} = 2.8 V; $V_{I(CTRL)}$ ≥ 0.8 V; T_{amb} = 25 °C; input matched to 50 Ω using a 4.7 nH inductor in series; Figure 4 unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gain mode						
I_{CC}	supply current	$V_{I(CTRL)}$ ≥ 0.8 V	-	4.4	-	mA
G_p	power gain	f = 1843 MHz [1]	-	17.0	-	dB
		f = 1960 MHz [2]	-	16.6	-	dB
		f = 2140 MHz [3]	-	15.8	-	dB
RL_{in}	input return loss	f = 1843 MHz [1]	-	6.0	-	dB
		f = 1960 MHz [2]	-	7.5	-	dB
		f = 2140 MHz [3]	-	9.5	-	dB
RL_{out}	output return loss	f = 1843 MHz [1]	-	15	-	dB
		f = 1960 MHz [2]	-	11.5	-	dB
		f = 2140 MHz [3]	-	8	-	dB
ISL	isolation	f = 1843 MHz [1]	-	25	-	dB
		f = 1960 MHz [2]	-	25	-	dB
		f = 2140 MHz [3]	-	25	-	dB
NF	noise figure	f = 1843 MHz [1][4]	-	0.75	-	dB
		f = 1960 MHz [2][4]	-	0.80	-	dB
		f = 2140 MHz [3][4]	-	0.85	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression	f = 1843 MHz [1]	-	−7.5	-	dBm
		f = 1960 MHz [2]	-	−6.5	-	dBm
		f = 2140 MHz [3]	-	−5.5	-	dBm
$IP3_i$	input third-order intercept point	f = 1843 MHz [1]	-	−1.0	-	dBm
		f = 1960 MHz [2]	-	−0.5	-	dBm
		f = 2140 MHz [3]	-	−1.0	-	dBm
t_{on}	turn-on time	time from $V_{I(CTRL)}$ ON, to 90 % of the gain	-	-	4	µs
t_{off}	turn-off time	time from $V_{I(CTRL)}$ OFF, to 10 % of the gain	-	-	1	µs
Bypass mode						
I_{CC}	supply current	$V_{I(CTRL)}$ < 0.3 V	-	-	1	µA
G_p	power gain	f = 1843 MHz [1]	-	−2.5	-	dB
		f = 1960 MHz [2]	-	−2.7	-	dB
		f = 2140 MHz [3]	-	−3.0	-	dB
RL_{in}	input return loss	f = 1843 MHz [1]	-	13	-	dB
		f = 1960 MHz [2]	-	12	-	dB
		f = 2140 MHz [3]	-	11.0	-	dB

Table 10. Characteristics *...continued*

1805 MHz ≤ f ≤ 2200 MHz; V_{CC} = 2.8 V; $V_{I(CTRL)}$ ≥ 0.8 V; T_{amb} = 25 °C; input matched to 50 Ω using a 4.7 nH inductor in series; Figure 4 unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
RL_{out}	output return loss	f = 1843 MHz	[1]	-	9.0	-	dB
		f = 1960 MHz	[2]	-	8.5	-	dB
		f = 2140 MHz	[3]	-	8.0	-	dB

[1] E_UTRA operating band 3 (1805 MHz to 1880 MHz).

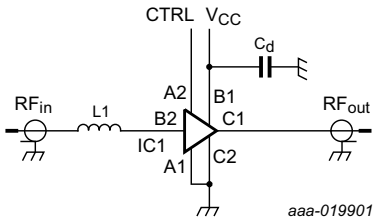
[2] E_UTRA operating band 2 (1930 MHz to 1990 MHz).

[3] E_UTRA operating band 1 (2110 MHz to 2170 MHz).

[4] PCB losses are subtracted

10. Application information

10.1 LTE LNA



For a list of components see Table 11.

Fig 4. Schematics LTE LNA evaluation board

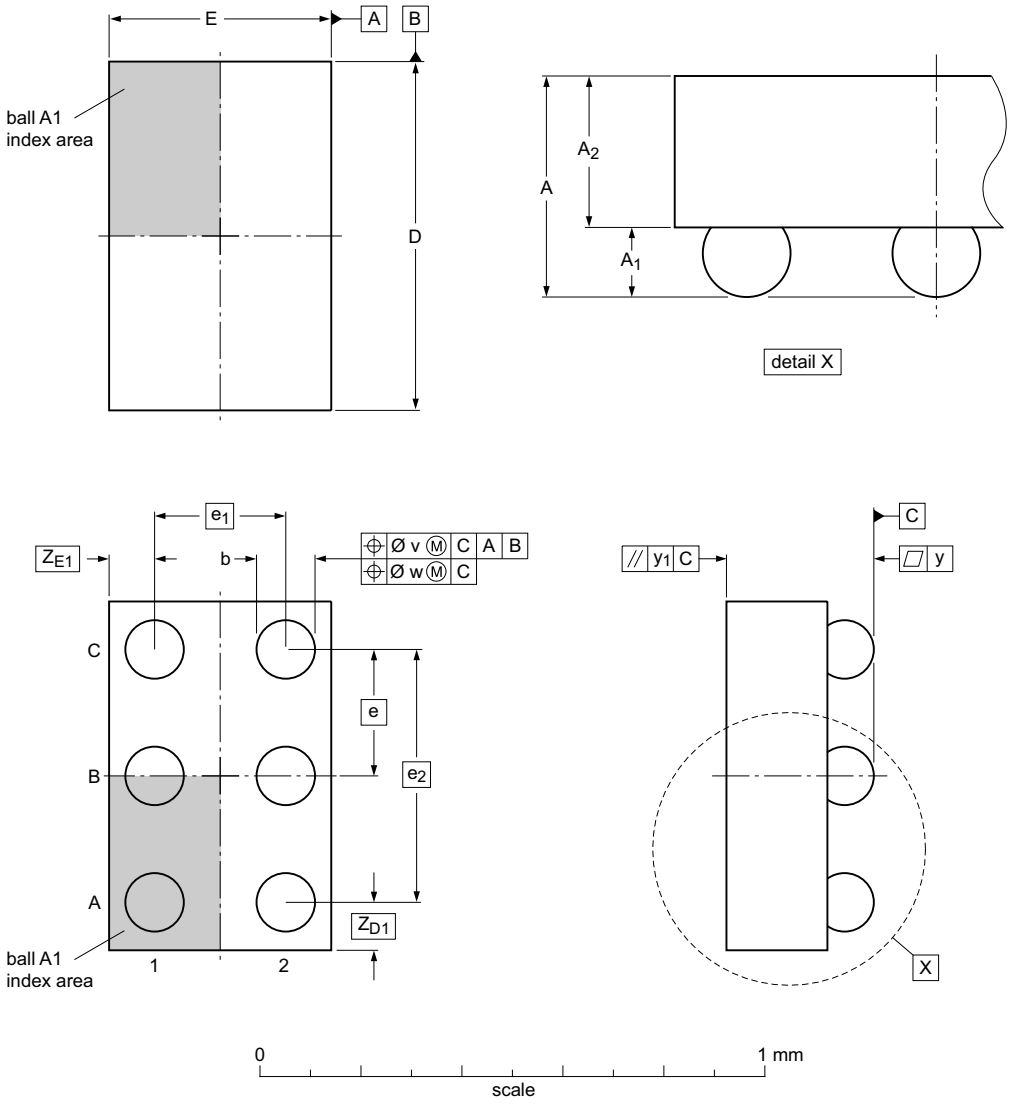
Table 11. List of components

For schematics see Figure 4

Component	Description	Value		Remarks
C_d	decoupling capacitor	1 uF		to suppress power supply noise
IC1	BGS8M4UK	-		NXP Semiconductors N.V.
L1	high-quality matching inductor	4.7 nH		Murata LQW15A

11. Package outline

WLCSP6: wafer level chip-scale package; 6 bumps; 0.69 x 0.44 x 0.29 mm **SOT1445-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1	Z_{D1}	Z_{E1}
	max	0.31	0.105	0.215	0.131	0.705	0.455								0.105	0.10
mm	nom	0.29	0.090	0.200	0.116	0.690	0.440	0.25	0.26	0.50	0.15	0.05	0.03	0.05	0.095	0.09
	min	0.27	0.075	0.185	0.101	0.675	0.425								0.085	0.08

sot1445-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1445-1						~~15-04-28~~ 15-05-11

Fig 5. Package outline SOT1445-1 (WLCSP6)

12. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

13. Mounting

This WLCSP is only to be used in an overmolded module (using MUF)

14. Abbreviations

Table 12. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
HBM	Human Body Model
LTE	Long Term Evolution
MMIC	Monolithic Microwave Integrated Circuit
MUF	Molded UnderFill
PCB	Printed-Circuit Board
SiGe:C	Silicon Germanium Carbon

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BGS8M4UK v.1	20151201	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Bare die — All die are tested on compliance with their related technical specifications as stated in this data sheet up to the point of wafer sawing and are handled in accordance with the NXP Semiconductors storage and transportation conditions. If there are data sheet limits not guaranteed, these will be separately indicated in the data sheet. There are no post-packing tests performed on individual die or wafers.

NXP Semiconductors has no control of third party procedures in the sawing, handling, packing or assembly of the die. Accordingly, NXP Semiconductors assumes no liability for device functionality or performance of the die or systems after third party sawing, handling, packing or assembly of the die. It is the responsibility of the customer to test and qualify their application in which the die is used.

All die sales are conditioned upon and subject to the customer entering into a written die sale agreement with NXP Semiconductors through its legal department.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

18. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 1 December 2015
Document identifier: BGS8M4UK