# Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1<sup>st</sup>, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)
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## MOS FIELD EFFECT TRANSISTOR

# $\mu$ PA672T

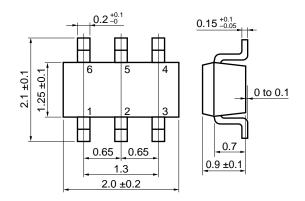
## N-CHANNEL MOS FET ARRAY FOR SWITCHING

The  $\mu$ PA672T is a super-mini-mold device provided with two MOS FET elements. It achieves high-density mounting and saves mounting costs.

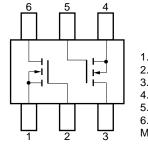
#### **FEATURES**

- Two MOS FET circuits in package the same size as SC-70
- · Automatic mounting supported

#### PACKAGE DIMENSIONS (in millimeters)



#### PIN CONNECTION



- 1. Source 1 (S1)
- 2. Gate 1 (G1) 3. Drain 2 (D2)
- 4. Source 2 (S2)
- 5. Gate 2 (G2)
- 6. Drain 1 (D1) Marking: MA

#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C)

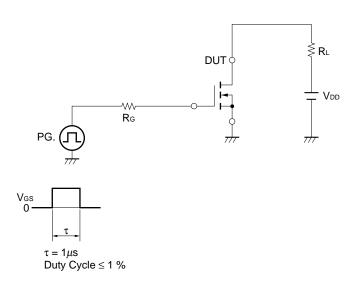
PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Drain to Source Voltage	VDSS		50	V
Gate to Source Voltage	Vgss		±7.0	V
Drain Current (DC)	I <sub>D(DC)</sub>		100	mA
Drain Current (pulse)	D(pulse)	PW ≤ 10 ms, Duty Cycle ≤ 50 %	200	mA
Total Power Dissipation	Рт		200 (Total)	mW
Channel Temperature	Tch		150	°C
Storage Temperature	T <sub>stg</sub>		-55 to +150	°C

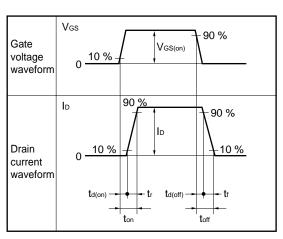


## ELECTRICAL CHARACTERISTICS (TA = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Cut-off Current	IDSS	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0			10	μΑ
Gate Leakage Current	Igss	$V_{GS} = \pm 7.0 \text{ V}, V_{DS} = 0$			±5.0	μΑ
Gate Cut-off Voltage	V <sub>GS(off)</sub>	$V_{DS} = 3.0 \text{ V}, \text{ ID} = 1.0 \ \mu\text{A}$	0.7	1.0	1.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 3.0 V, I <sub>D</sub> = 10 mA	20			mS
Drain to Source On-State Resistance	RDS(on)1	Vgs = 2.5 V, ID = 10 mA		20	40	Ω
Drain to Source On-State Resistance	RDS(on)2	V <sub>G</sub> S = 4.0 V, I <sub>D</sub> = 10 mA		15	20	Ω
Input Capacitance	Ciss	V <sub>DS</sub> = 3.0 V, V <sub>GS</sub> = 0, f = 1.0 MHz		6		pF
Output Capacitance	Coss			8		pF
Reverse Transfer Capacitance	Crss			1.2		pF
Turn-On Delay Time	td(on)	$V_{DD} = 3 \text{ V, ID} = 20 \text{ mA, V}_{GS(on)} = 3 \text{ V,}$ $R_G = 10 \Omega, R_L = 120 \Omega$		9		ns
Rise Time	tr			50		ns
Turn-Off Delay Time	td(off)			20		ns
Fall Time	t <sub>f</sub>			40		ns

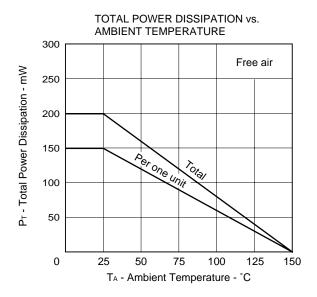
## SWITCHING TIME MEASUREMENT CIRCUIT AND CONDITIONS

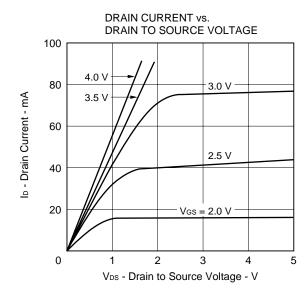


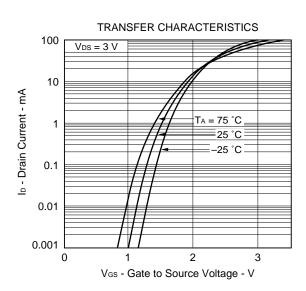


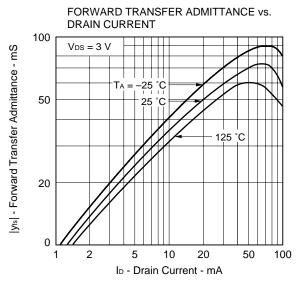


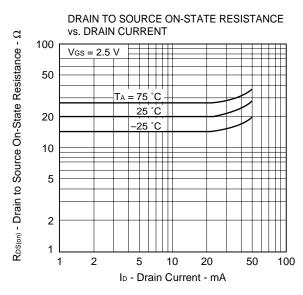
### TYPICAL CHARACTERISTICS (TA = 25 °C)

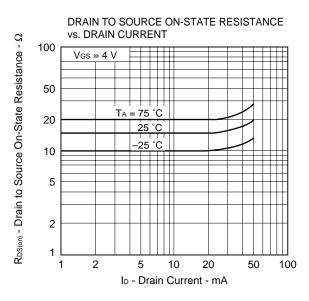




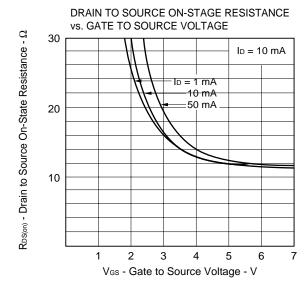


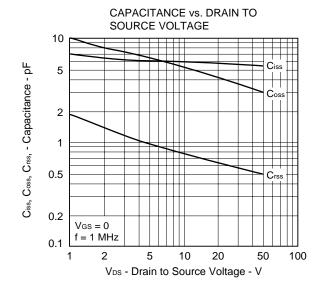


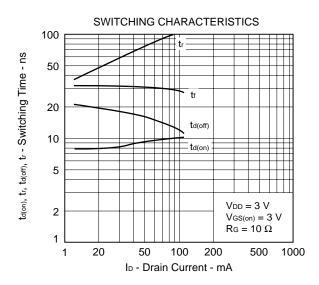


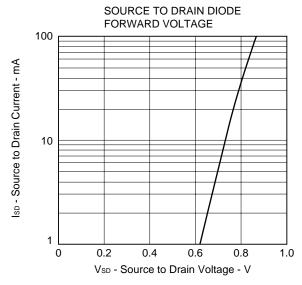














## REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	C10535E
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	X10679E

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