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December 2013

# **FCD7N60**

# N-Channel SuperFET<sup>®</sup> MOSFET 600 V, 7 A, 600 m $\Omega$

#### **Features**

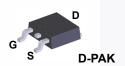
- 650 V @ T<sub>.1</sub> = 150°C
- Typ.  $R_{DS(on)}$  = 530 m $\Omega$
- Ultra Low Gate Charge (Typ. Q<sub>q</sub> = 23 nC)
- Low Effective Output Capacitance (Typ. C<sub>oss(eff.)</sub> = 60 pF)
- · 100% Avalanche Tested
- · RoHS Compliant

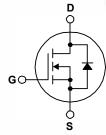
### **Application**

- · LCD / LED TV and Monitor
- Lighting
- · Solar Inverter
- · AC-DC Power Supply

## **Description**

SuperFET® MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low onresistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.





# **MOSFET Maximum Ratings** $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter		FCD7N60TM / FCD7N60TM_WS	Unit
V <sub>DSS</sub>	Drain to Source Voltage		600	V
	- Continuous (T <sub>C</sub> = 25°C)		7	^
ID	Drain Current	- Continuous (T <sub>C</sub> = 100°C)	4.4	A
$I_{DM}$	Drain Current	- Pulsed (Not	te 1) 21	Α
V <sub>GSS</sub>	Gate to Source Voltage		±30	V
E <sub>AS</sub>	Single Pulsed Avalanche Ener	gy (Not	te 2) 230	mJ
I <sub>AR</sub>	Avalanche Current	(Not	te 1) 7	Α
E <sub>AR</sub>	Repetitive Avalanche Energy	(Not	te 1) 8.3	mJ
dv/dt	Peak Diode Recovery dv/dt	(Not	te 3) 20	V/ns
D	Davisa Diagination	$(T_C = 25^{\circ}C)$	83	W
$P_{D}$	Power Dissipation	- Derate Above 25°C	0.67	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150	οС
T <sub>L</sub>	Maximum Lead Temperature f	or Soldering, 1/8" from Case for 5 Seconds	s 300	°C

#### **Thermal Characteristics**

Symbol	Parameter	FCD7N60TM / FCD7N60TM_WS	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	83	- 0/00

# **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCD7N60TM	FCD7N60	D-PAK	Tape and Reel	330 mm	16 mm	2500 units
FCD7N60TM_WS	FCD7N60	D-PAK	Tape and Reel	330 mm	16 mm	2500 units

# **Electrical Characteristics** $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV <sub>DSS</sub> Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}, T_C = 25^{\circ}\text{C}$	600	-	-	V	
	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}, T_C = 150^{\circ}\text{C}$	-	650	-	V	
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	-	0.6	-	V/°C
BV <sub>DS</sub>	Drain to Source Avalanche Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 7.0 A	-	700	-	V
	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	-	-	1	^
DSS		$V_{DS} = 480 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	-	10	μΑ
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0 V	-	-	±100	nA

#### On Characteristics

V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	3.0	-	5.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS}$ = 10 V, $I_{D}$ = 3.5 A	-	0.53	0.6	Ω
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 40 \text{ V}, I_{D} = 3.5 \text{ A}$	-	6	ı	S

### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V - 25 V V - 0 V	-	710	920	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	380	500	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 1/11/2	-	34	-	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	22	29	pF
C <sub>oss(eff.)</sub>	Effective Output Capacitance	$V_{DS} = 0 V \text{ to } 400 V, V_{GS} = 0 V$	-	60	-	pF

#### **Switching Characteristics**

•							
t <sub>d(on)</sub>	Turn-On Delay Time			-	35	80	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{DD}$ = 300 V, $I_{D}$ = 7.0 A, $V_{GS}$ = 10 V , $R_{G}$ = 25 $\Omega$		- /	55	120	ns
$t_{d(off)}$	Turn-Off Delay Time			-	75	160	ns
t <sub>f</sub>	Turn-Off Fall Time		(Note 4)		32	75	ns
Q <sub>g(tot)</sub>	Total Gate Charge at 10V	V <sub>DS</sub> = 480 V, I <sub>D</sub> = 7.0 A,		-	23	30	nC
$Q_{gs}$	Gate to Source Gate Charge	V <sub>GS</sub> = 10 V		-	4.2	5.5	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		(Note 4)	-	11.5	-	nC

#### **Drain-Source Diode Characteristics**

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	7	Α
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current		-	-	21	Α
$V_{SD}$	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 7.0 A	-	-	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 7.0 A,	-	360	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	$V_{GS} = 0 \text{ V, } I_{SD} = 7.0 \text{ A,}$ $dI_F/dt = 100 \text{ A/}\mu\text{s}$	-	4.5	-	μС

- 1. Repetitive rating: pulse-width limited by maximum junction temperature.
- 2. I<sub>AS</sub> = 3.5 A, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25  $\Omega$ , starting T<sub>J</sub> = 25°C.
- 3.  $I_{SD} \le 7$  A, di/dt  $\le 200$  A/ $\mu$ s,  $V_{DD} \le BV_{DSS}$ , starting  $T_J$  = 25°C.
- 4. Essentially independent of operating temperature typical characteristics.

# **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

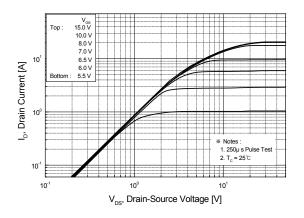


Figure 2. Transfer Characteristics

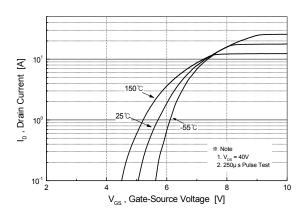


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

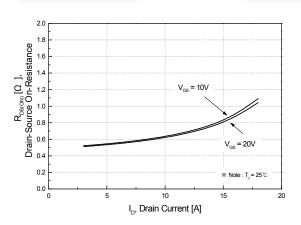


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

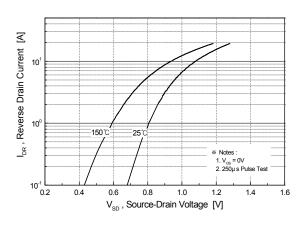


Figure 5. Capacitance Characteristics

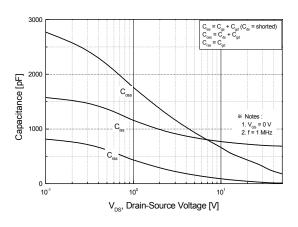
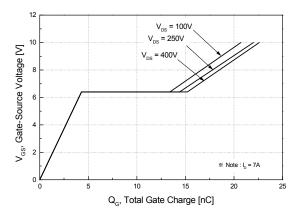


Figure 6. Gate Charge Characteristics



# **Typical Performance Characteristics** (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

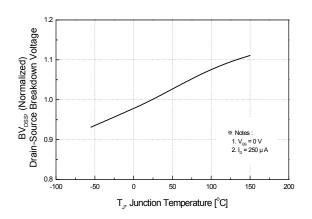


Figure 8. On-Resistance Variation vs. Temperature

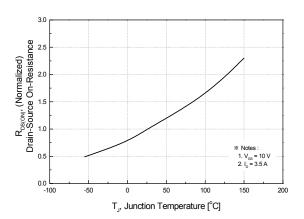


Figure 9. Maximum Safe Operating Area

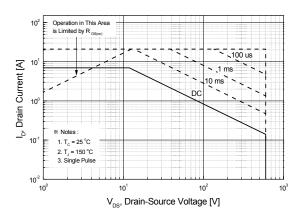


Figure 10. Maximum Drain Current vs. Case Temperature

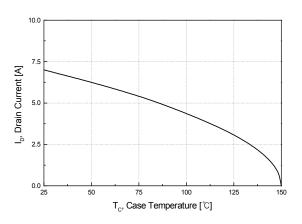
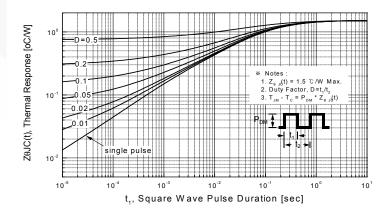


Figure 11. Transient Thermal Response Curve



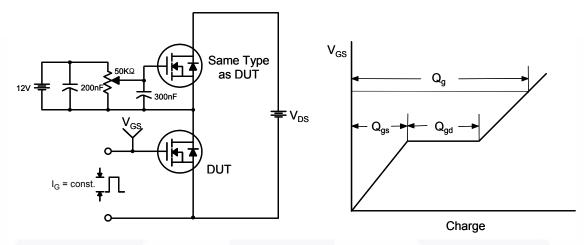


Figure 12. Gate Charge Test Circuit & Waveform

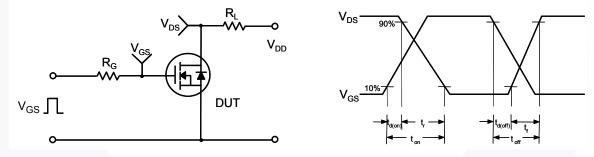


Figure 13. Resistive Switching Test Circuit & Waveforms

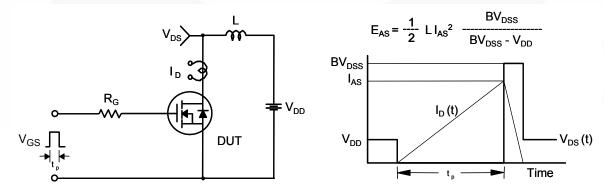


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

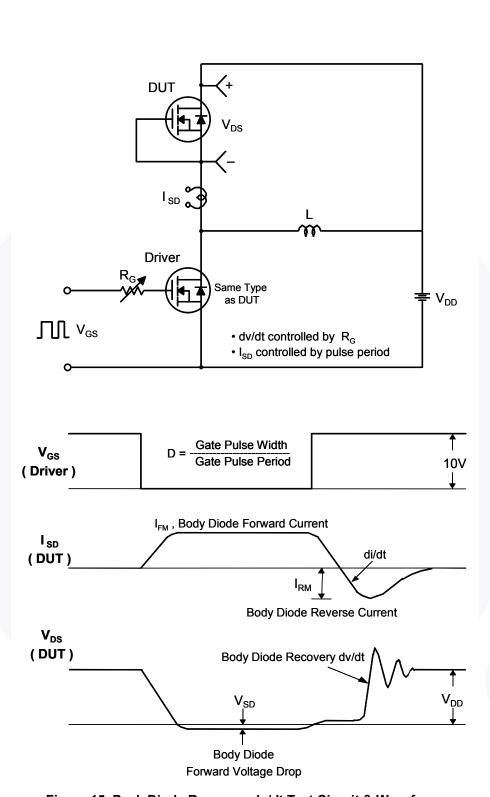


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

#### **Mechanical Dimensions**

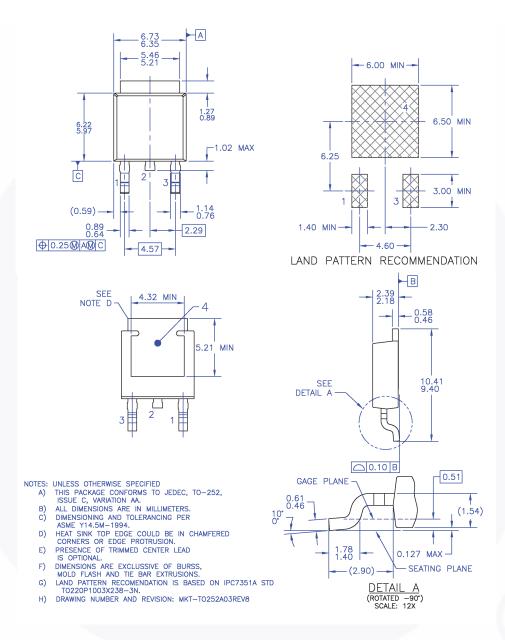


Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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